CLAIMS

What is claimed is:

1. A semiconductor device assembly comprising:

a substrate having a surface, having a layer comprising substantially diamond provided over at least a portion of said surface of said substrate having at least one aperture therein, and having at least one contact pad having a periphery, said at least one contact pad having at least a portion thereof extending at least partially over said layer comprising substantially diamond adjacent the at least one aperture therein and having at least a portion thereof extending through the at least one aperture in said layer comprising substantially diamond connected to at least one circuit on said substrate.

2. The assembly according to claim 1, wherein the periphery of said at least one contact pad covers portions of said layer comprising substantially diamond adjacent the at least one aperture therein.

3. The assembly according to claim 1, further comprising a conductive bump deposited on said at least one contact pad.

4. The assembly according to claim 1, further comprising:

a passivation layer located between said substrate and said layer comprising substantially diamond.

5. The assembly according to claim 4, wherein said passivation layer has at least one trace having at least a portion thereof located on a portion of said passivation layer to connect said substrate and said at least one contact pad.

6. The assembly according to claim 4, wherein said passivation layer comprises a polyimide.

7. The assembly according to claim 1, wherein said layer comprising substantially diamond having a thickness of at least about 50 angstroms.

8. The assembly according to claim 1, wherein said layer comprising substantially diamond having a thickness between about 50 to 2000 angstroms.

9. The assembly according to claim 1, further comprising:
a second layer comprising substantially diamond located between said substrate and said layer comprising substantially diamond.

10. The assembly according to claim 9, wherein at least one of said layer comprising substantially diamond and said second layer comprising substantially diamond has at least a portion of one trace located on a portion thereof to connect said substrate and said at least one contact pad.

11. The assembly according to claim 9, further comprising:
a passivation layer located between said layer comprising substantially diamond and said second layer comprising substantially diamond.

12. The assembly according to claim 11, wherein said passivation layer has at least a portion of at least one trace located thereon to connect said substrate and said at least one contact pad.

13. The assembly according to claim 5, further comprising:
a film comprising diamond formed between said passivation layer and said substrate, said substantially diamond film directly contacting said surface of said substrate.

14. The assembly according to claim 1, wherein said layer comprising substantially diamond comprises substantially polycrystalline diamond.

15. The assembly according to claim 1, wherein said layer comprising substantially diamond comprises substantially amorphous diamond.

16. The assembly according to claim 1, wherein said layer comprising substantially diamond comprises polycrystalline diamond and amorphous diamond.

17. The assembly according to claim 1, wherein said layer comprising substantially diamond includes one of polycrystalline diamond and amorphous diamond and another material.

18. The assembly according to claim 1, wherein said layer comprising substantially diamond includes polycrystalline diamond and amorphous diamond and another material.

19. The assembly according to claim 1, wherein said substrate comprises: a semiconductor die.

20. The assembly according to claim 1, wherein said substrate comprises: a bare semiconductor die.

21. The assembly according to claim 1, wherein said substrate comprises: a semiconductor wafer.

22. The assembly according to claim 1, wherein said substrate comprises: a portion of a semiconductor wafer.

23. The assembly according to claim 1, wherein said substrate comprises: a carrier substrate.

24. The assembly according to claim 1, wherein said substrate comprises: a carrier substrate for a flip-chip semiconductor device assembly.

25. The assembly according to claim 1, wherein said substrate comprises:
a carrier substrate having a semiconductor die attached thereto.

26. The assembly according to claim 1, wherein said substrate comprises:
a carrier substrate having a semiconductor die adhesively attached thereto.

27. A semiconductor die assembly comprising:
a substrate having a surface, a layer having at least one aperture therein, said layer including diamond provided substantially over said surface of said substrate, and at least one contact pad having at least a portion thereof extending at least partially over said layer and having a portion extending at least into the at least one aperture in said layer.

28. The assembly according to claim 27, wherein said at least one contact pad has substantially a periphery thereof contacting said layer.

29. The assembly according to claim 27, further comprising:
a conductive bump located on said at least one contact pad.

30. The assembly according to claim 27, further comprising:
a passivation layer provided between said substrate and said layer.

31. The assembly according to claim 30, wherein said passivation layer carries at least one trace to electrically connect said substrate and said at least one contact pad.

32. The assembly according to claim 30, wherein said passivation layer comprises a polyimide.

33. The assembly according to claim 27, wherein said layer has a thickness of at least about 50 angstroms.

34. The assembly according to claim 27, wherein said layer has a thickness of between about 50 to 2000 angstroms.

35. The assembly according to claim 27, further comprising:
a second layer including diamond located between said substrate and said layer.

36. The assembly according to claim 35, wherein at least one of said layer and said second layer having at least one trace connecting said substrate and said at least one contact pad.

37. The assembly according to claim 35, further comprising:
a passivation layer between said layer and said second layer.

38. The assembly according to claim 37, wherein said passivation layer having at least one trace connecting said substrate and said at least one contact pad.

39. The assembly according to claim 31, further comprising:
a film including diamond formed between said passivation layer and said substrate, said film contacting said surface of said substrate.

40. A heat sink disposed on a substrate comprising:
a layer including diamond disposed on at least a portion of a surface of a substrate, said layer including at least one opening therein; and
at least one pad located on at least a portion of said surface of the substrate, said at least one pad having a portion thereof extending over at least a portion of said layer and having a portion thereof located in said at least one opening.

41. The heat sink according to claim 40, wherein said at least one pad having more than one portion thereof extending over said at least said portion of said layer.

42. The heat sink according to claim 40, further comprising:
a passivation layer provided between the substrate and said layer.

43. The heat sink according to claim 42, wherein said passivation layer has at least one trace connecting the substrate and said at least one pad.

44. The heat sink according to claim 40, further comprising:
a second layer including diamond located between said substrate and said layer.

45. The heat sink according to claim 44, wherein at least one of said layer and said second layer has at least one trace connecting said substrate and said at least one pad.

46. The heat sink according to claim 44, further comprising:
a passivation layer between said layer and said second layer.

47. The heat sink according to claim 46, wherein said passivation layer has at least one trace connecting said substrate and said at least one pad.

48. The heat sink according to claim 42, further comprising:
a film including diamond formed between said passivation layer and said substrate, said film contacting the substrate.

49. A semiconductor device assembly comprising:
a semiconductor device having an active surface, having a layer comprising substantially diamond provided over at least a portion of said active surface of said substrate having at least one aperture therein, and having at least one bond pad having a periphery located on said active surface, said at least one bond pad having at least a portion thereof extending at least partially over said layer comprising substantially diamond adjacent the at least one aperture therein and having at least a portion thereof extending at least through a

portion of the at least one aperture in said layer comprising substantially diamond, said at least one bond pad connected to at least one circuit on said semiconductor device; and a substrate.

50. The assembly according to claim 49, wherein the periphery of said at least one bond pad covers portions of said layer adjacent the at least one aperture therein.

51. The assembly according to claim 49, further comprising:
a conductive bump deposited on said at least one bond pad.

52. The assembly according to claim 49, further comprising:
a passivation layer located between said semiconductor device and said layer comprising substantially diamond.

53. The assembly according to claim 52, wherein said passivation layer has at least one trace having at least a portion thereof located on a portion of said passivation layer to connect said semiconductor device and said at least one bond pad.

54. The assembly according to claim 52, wherein said passivation layer comprises a polyimide.

55. The assembly according to claim 49, wherein said layer comprising substantially diamond has a thickness of at least about 50 angstroms.

56. The assembly according to claim 49, wherein said layer comprising substantially diamond has a thickness between about 50 and 2000 angstroms.

57. The assembly according to claim 49, further comprising:
a second layer comprising substantially diamond located between said semiconductor device and said layer comprising substantially diamond.

58. The assembly according to claim 57, wherein one of said at least one of said layer comprising substantially diamond and said second layer comprising substantially diamond has at least a portion of one trace located on a portion thereof to connect said substrate and said at least one bond pad.

59. The assembly according to claim 57, further comprising:
a passivation layer located between said layer comprising substantially diamond and said second layer comprising substantially diamond.

60. The assembly according to claim 59, wherein said passivation layer has at least a portion of at least one trace located thereon to connect said substrate and said at least one bond pad.

61. The assembly according to claim 53, further comprising:
a film comprising diamond formed between said passivation layer and said substrate, said film directly contacting said active surface of said substrate.

62. The assembly according to claim 49, wherein said layer comprising substantially diamond comprises substantially polycrystalline diamond.

63. The assembly according to claim 49, wherein said layer comprising substantially diamond comprises substantially amorphous diamond.

64. The assembly according to claim 49, wherein said layer comprising substantially diamond comprises polycrystalline diamond and amorphous diamond.

65. The assembly according to claim 49, wherein said layer comprising substantially diamond includes one of polycrystalline diamond, amorphous diamond, and another material.

66. The assembly according to claim 49, wherein said layer comprising substantially diamond includes polycrystalline diamond and amorphous diamond and another material.

67. The assembly according to claim 49, wherein said semiconductor device comprises:
a semiconductor die.

68. The assembly according to claim 49, wherein said semiconductor device comprises:
a bare semiconductor die.

69. The assembly according to claim 49, wherein said semiconductor device comprises:
a semiconductor wafer.

70. The assembly according to claim 49, wherein said semiconductor device comprises:
a portion of a semiconductor wafer.

71. The assembly according to claim 49, wherein said semiconductor device comprises:
a flip-chip semiconductor die.

72. The assembly according to claim 49, wherein said substrate comprises:
a carrier substrate for a flip-chip semiconductor device assembly.

73. The assembly according to claim 49, wherein said substrate comprises:
a carrier substrate having a semiconductor die attached thereto.

74. The assembly according to claim 67, wherein said substrate comprises:
a carrier substrate having said semiconductor die adhesively attached thereto.

75. A semiconductor die assembly comprising:
a semiconductor die having an active surface, a layer having at least one aperture therein, said layer including diamond provided substantially over a portion of said active surface of said substrate, and at least one bond pad having at least a portion thereof extending at least partially over said layer and having a portion extending at least into the at least one aperture in said layer; and
a substrate having said semiconductor die attached thereto.

76. The assembly according to claim 75, wherein said at least one bond pad has substantially a periphery thereof contacting said layer.

77. The assembly according to claim 75, further comprising:
a conductive bump located on said at least one bond pad.

78. The assembly according to claim 75, further comprising:
a passivation layer provided between said semiconductor die and said layer.

79. The assembly according to claim 78, wherein said passivation layer having at least one trace connecting said semiconductor die and said at least one bond pad.

80. The assembly according to claim 78, wherein said passivation layer comprises a polyimide.

81. The assembly according to claim 75, wherein said layer has a thickness of at least about 50 angstroms.

82. The assembly according to claim 75, wherein said layer has a thickness between about 50 and 2000 angstroms.

83. The assembly according to claim 75, further comprising:
a second layer including diamond located between said semiconductor die and said layer.

84. The assembly according to claim 83, wherein at least one of said layer and said second layer having at least one trace connecting said semiconductor die and said at least one bond pad.

85. The assembly according to claim 84, further comprising:
a passivation layer between said layer and said second layer.

86. The assembly according to claim 85, wherein said passivation layer having at least one trace connecting said substrate and said at least one bond pad.

87. The assembly according to claim 78, further comprising:
a film including diamond formed between said passivation layer and said semiconductor die, said film contacting said active surface of said semiconductor die.

88. A heat sink disposed on a semiconductor device comprising:
a layer including diamond disposed on at least a portion of a surface of a semiconductor device, said layer including at least one opening therein; and
at least one bond pad located on at least a portion of an active surface of the semiconductor device, said at least one bond pad having a portion thereof extending over at least a portion of said layer and having another portion thereof located in said at least one opening.

89. The heat sink according to claim 88, wherein said at least one bond pad having more than one portion thereof extending over said at least a portion of said layer.

90. The heat sink according to claim 88, further comprising:
a passivation layer provided between the semiconductor device and said layer.

91. The heat sink according to claim 90, wherein said passivation layer has at least one trace connecting the semiconductor device and said at least one bond pad.

92. The heat sink according to claim 88, further comprising:
a second layer including diamond located between said semiconductor device and said layer.

93. The heat sink according to claim 92, wherein at least one of said layer and said second layer has at least one trace connecting said substrate and said at least one bond pad.

94. The heat sink according to claim 92, further comprising:
a passivation layer between said layer and said second layer.

95. The heat sink according to claim 94, wherein said passivation layer has at least one trace connecting said semiconductor device and said at least one bond pad.

96. The heat sink according to claim 90, further comprising:
a film including diamond formed between said passivation layer and said semiconductor device, said film contacting the substrate.

97. A semiconductor die comprising:
a substrate having a surface, at least one circuit located on said substrate, a layer including diamond provided over at least a portion of said surface of said substrate having at least one aperture therein, and having at least one contact pad having a periphery, said at least one contact pad having at least a portion thereof extending at least partially over said

layer adjacent the at least one aperture therein and having at least a portion thereof extending through the at least one aperture in said layer, said at least one contact pad connected to the at least one circuit on said substrate.

98. The semiconductor die according to claim 97, wherein the periphery of said at least one contact pad covers portions of said layer adjacent the at least one aperture therein.

99. The semiconductor die according to claim 97, further comprising:
a conductive bump deposited on said at least one contact pad.

100. The semiconductor die according to claim 97, further comprising:
a passivation layer located between said substrate and said layer.

101. The semiconductor die according to claim 100, wherein said passivation layer has at least one trace having at least a portion thereof located on a portion of said passivation layer to connect said substrate and said at least one contact pad.

102. The semiconductor die according to claim 100, wherein said passivation layer comprises a polyimide.

103. The semiconductor die according to claim 97, wherein said layer has a thickness of at least about 50 angstroms.

104. The semiconductor die according to claim 97, wherein said layer has a thickness of between about 50 and 2000 angstroms.

105. The semiconductor die according to claim 97, further comprising:
a second layer including diamond located between said substrate and said layer.

106. The semiconductor die according to claim 105, wherein one of said at least one of said layer and said second layer has at least a portion of one trace located on a portion thereof to connect said substrate and said at least one contact pad.

107. The semiconductor die according to claim 105, further comprising:
a passivation layer located between said layer and said second layer.

108. The semiconductor die according to claim 107, wherein said passivation layer has at least a portion of at least one trace located thereon to connect said substrate and said at least one contact pad.

109. The semiconductor die according to claim 101, further comprising:
a film including diamond formed between said passivation layer and said substrate, said film directly contacting said surface of said substrate.

110. The semiconductor die according to claim 97, wherein said layer comprises substantially polycrystalline diamond.

111. The semiconductor die according to claim 97, wherein said layer comprises substantially amorphous diamond.

112. The semiconductor die according to claim 97, wherein said layer comprises polycrystalline diamond and amorphous diamond.

113. The semiconductor die according to claim 97, wherein said layer includes one of polycrystalline diamond and amorphous diamond and another material.

114. The semiconductor die according to claim 97, wherein said layer includes polycrystalline diamond and amorphous diamond and another material.

115. The semiconductor die according to claim 97, wherein said substrate comprises:

a semiconductor wafer.

116. The semiconductor die according to claim 97, wherein said substrate comprises:

a portion of a semiconductor wafer.

117. A computer assembly comprising:

at least one input device;

at least one output device;

at least one microprocessor connected to said at least one input device and said at least one output device; and

a substrate connected to said at least one microprocessor, said substrate having a surface, at least one circuit located on said substrate, a layer including diamond provided over at least a portion of said surface of said substrate having at least one aperture therein, and having at least one contact pad having a periphery, said at least one contact pad having at least a portion thereof extending at least partially over said layer adjacent the at least one aperture therein and having at least a portion thereof extending through the at least one aperture in said layer connected to the at least one circuit on said substrate.

118. The computer assembly according to claim 117, wherein the periphery of said at least one contact pad covers portions of said layer adjacent the at least one aperture therein.

119. The computer assembly according to claim 117, further comprising:

a conductive bump deposited on said at least one contact pad.

120. The computer assembly according to claim 117, further comprising:

a passivation layer located between said substrate and said layer.

121. The computer assembly according to claim 120, wherein said passivation layer has at least one trace having at least a portion thereof located on a portion of said passivation layer to connect said substrate and said at least one contact pad.

122. The computer assembly according to claim 120, wherein said passivation layer comprises a polyimide.

123. The computer assembly according to claim 117, wherein said layer has a thickness of at least about 50 angstroms.

124. The computer assembly according to claim 117, wherein said layer has a thickness between about 50 to 2000 angstroms.

125. The computer assembly according to claim 117, further comprising:
a second layer including diamond located between said substrate and said layer.

126. The computer assembly according to claim 125, wherein one of said at least one of said layer and said second layer has at least a portion of one trace located on a portion thereof to connect said substrate and said at least one contact pad.

127. The computer assembly according to claim 125, further comprising:
a passivation layer located between said layer and said second layer.

128. The computer assembly according to claim 127, wherein said passivation layer has at least a portion of at least one trace located thereon to connect said substrate and said at least one contact pad.

129. The computer assembly according to claim 120, further comprising:
a film including diamond formed between said passivation layer and said substrate, said film directly contacting said surface of said substrate.

130. The computer assembly according to claim 117, wherein said layer comprises substantially polycrystalline diamond.

131. The computer assembly according to claim 117, wherein said layer comprises substantially amorphous diamond.

132. The computer assembly according to claim 117, wherein said layer comprises polycrystalline diamond and amorphous diamond.

133. The computer assembly according to claim 117, wherein said layer includes one of polycrystalline diamond and amorphous diamond and another material.

134. The computer assembly according to claim 117, wherein said layer includes polycrystalline diamond and amorphous diamond and another material.

135. The computer assembly according to claim 117, wherein said substrate comprises:
a semiconductor wafer.

136. The computer assembly according to claim 117, wherein said substrate comprises:
a portion of a semiconductor wafer.